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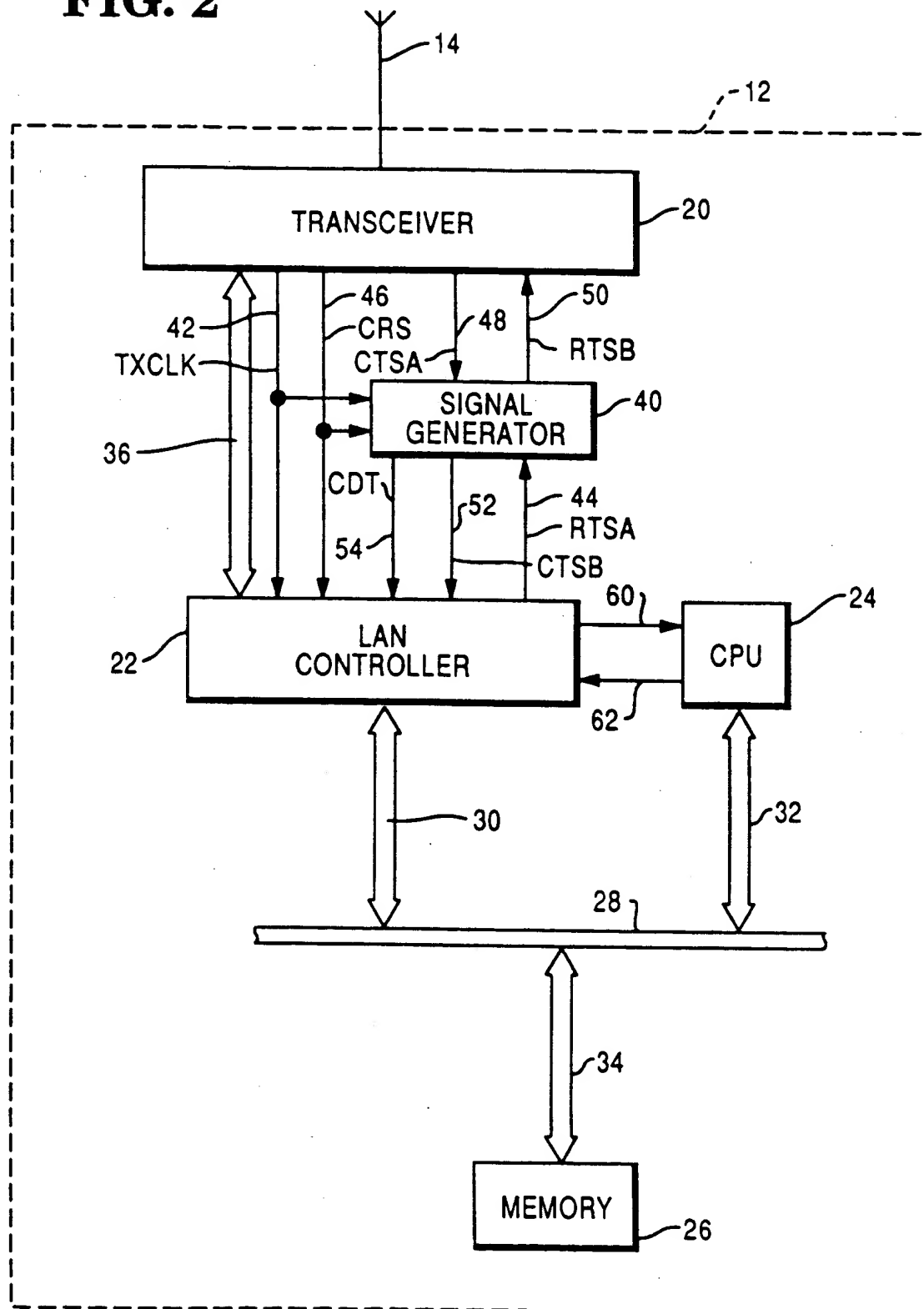
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(54) **Local area network having a wireless transmission link.**

(57) A local area network station (12) includes a transceiver (20) adapted to transmit and receive signals over a wireless communications link. The transceiver (20) is coupled to a CSMA/CD LAN controller device (22) and to a signal generator circuit (40) which is also coupled to the LAN controller device (22). If the station (12) desires to transmit a data frame but a carrier sense signal (CRS) indicates that the link is busy, transmission of the data frame is deferred, and after the carrier sense signal (CRS) becomes inactive, a collision is simulated by the signal generator circuit (40) providing a CDT signal to the LAN controller device (22) which goes into a backoff mode and attempts to retransmit the frame after a random backoff time. Thus, commercially available CSMA/CD chips can be utilized in a single wireless channel LAN environment using a CSMA/CA protocol, with a low risk of collisions.

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FIG. 2



This invention relates to local area networks (LANs) wherein a plurality of stations communicate with one another over a transmission medium for the transmission of digital data.

Various methods are known for sharing network communication channels or links among stations in a local area network. One widely used method is known as CSMA/CD, (carrier sense multiple access with collision detection). According to this known method, a station wishing to transmit a message listens until the transmission channel is idle before commencing to transmit an information packet. Furthermore, the station continues to listen to the channel after commencing a transmission and if a collision is detected, that is, more than one station has commenced to transmit an information packet, any station which detects such collision terminates its message transmission and transmits a jam pattern (or garble) such that all other stations can be informed of the collision, terminate message transmission, and wait a random time before attempting to commence a further message transmission.

The CSMA/CD protocol is the subject of an international (ISO) standard and corresponding IEEE Standard, No. 802.3, and has become a generally used protocol for LANs utilizing wired connections for transmission between the stations. In consequence, CSMA/CD LAN controller chips have become widely commercially available. Several manufacturers produce such chips, complying with the IEEE 802.3 standard. An example is the Intel 82586 LAN coprocessor chip, available from Intel Corporation of Santa Clara, California, USA. Such chips provide various facilities useful in LANs such as data rate range and backoff algorithm and configurable parameters such as slot time duration, retry counter offset and limit, and inter-frame spacing time.

However, LANs using wired interconnections have the disadvantage that extensive cabling is required to interconnect the stations. The provision of such cabling is generally inconvenient and gives rise to inflexibility if it is desired to alter the physical locations of the stations. It has been proposed to utilize a wireless transmission link operating at radio frequencies to replace the cabling interconnections of a LAN. However, if only a single radio channel is to be utilized for such a LAN, the widely accepted CSMA/CD protocol cannot generally be applied since a station cannot generally receive (or listen) while it is transmitting.

European Patent Application No. 0 064 818 discloses a wired LAN which utilizes a data collision avoidance method. Each station with a data packet ready for transmission monitors the activity of the communications channel. If activity on the channel is detected, the station waits until the channel is idle and then introduces a random wait, at the end of which the transmission is effected if the channel is still idle.

It is an object of the present invention to provide a method for operating a LAN (local area network) suitable for use with a single channel wireless transmission link, which provides a low risk of collisions on the transmission link, while enabling the use of LAN stations having a simple and inexpensive construction.

Therefore, according to one aspect of the present invention, there is provided a method of communicating among at least two data processing stations coupled by a wireless LAN operating over a wireless transmission channel, characterized by the steps of: providing a controller chip which is designed for use with a CSMA/CD protocol in a wired LAN; generating a control signal at a predetermined time by a data processing station wishing to transmit; using said control signal to activate a collision detect input of said controller chip; and using a random delay time determined in said controller chip to initiate transmission by said data processing station wishing to transmit.

According to a second aspect of the present invention, there is provided a local area network station, including memory means adapted to store data to be transmitted, and communication controller means adapted to control the transmission of data frames by said station; and transceiver means, characterized in that said transceiver means is adapted to operate on a single wireless transmission channel, in that said communication controller means is adapted to defer transmission of a data frame in response to a first control signal applied thereto and is further effective, in response to a second control signal applied thereto, to terminate the transmission of a data frame which is being transmitted and to reinitiate transmission thereof after a backoff period; and in that signal generating means is provided, coupled to said transceiver means and to said communication controller means and adapted, in response to the outputting by said communication controller means of a third control signal requesting transmission of a deferred data frame, to generate said second control signal thereby causing said communication controller means to inhibit transmission of the deferred data frame until said backoff period has elapsed.

It will be appreciated that a local area network station according to the second aspect of the invention has a simple construction and is suitable for a single channel wireless transmission link, resulting from the ability to use commercially available CSMA/CD controller chips as communication controller means and the utilization of such chips in a CSMA protocol with collision avoidance (CSMA/CA) rather than collision detection (CSMA/CD).

One embodiment of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:-

Fig. 1 is a diagram of a wireless LAN.

Fig. 2 is a block diagram of a typical station

utilized in the LAN shown in Fig. 1.

Fig. 3A and 3B taken together show a signal generating means used with this invention.

Figs. 4A, 4B and 4C are waveform diagrams helpful in understanding the operation of the LAN station shown in Fig. 2, with Fig. 4C being shown on the sheet containing Fig. 1.

Referring first to Fig. 1, there is shown a wireless local area network (LAN) 10 including a plurality N of data processing stations 12, shown individually as 12-1 to 12-N. Each station has an antenna 14, shown individually as 14-1 to 14-N. Although only a single antenna is shown for each station, it will be understood that each station may have two antennas to provide a diversity feature for alleviating multipath fading which may arise in some environments.

Communication among the stations 12 takes place over a radio frequency link, on a single radio channel, and preferably uses spread spectrum communication technology.

Referring now to Fig. 2, there is shown a block diagram of the components of a typical station 12, illustrating the blocks thereof which are pertinent to the present invention. The station 12 includes a transceiver 20, a LAN controller 22, a central processor unit (CPU) 24, and a memory 26. A local bus 28 is connected to the LAN controller 22 by a bus 30, to the CPU 24 by a bus 32, and to the memory 26 by a bus 34. The LAN controller 22 is a commercially available LAN controller device, suitable for the CSMA/CD (carrier sense multiple access with collision detection) protocol. In the preferred embodiment, the LAN controller 22 is an Intel 82586 LAN coprocessor chip, available from Intel Corporation of Santa Clara, California, U.S.A.

The transceiver 20 and LAN controller 22 are interconnected by a bus 36 which carries data and control signals. Also included in the station 12 is a signal generator circuit 40 which is interposed between the transceiver 20 and the LAN controller 22. The signal generator circuit 40 receives transmit clock pulses TXCLK from the transceiver 20 over line 42 and a request-to-send signal RTSA from the LAN controller 22 over a line 44.

The signal generator circuit 40 also receives a carrier sense signal CRS and a clear-to-send signal CTSA from the transceiver 20 over lines 46, 48 respectively. The TXCLK pulses on the line 42 and the CRS signal on the line 46 are also applied directly to the LAN controller 22.

The signal generator circuit 40 provides an output request-to-send signal RTSB over a line 50 connected to the transceiver 20, an output clear-to-send signal CTSB over a line 52 connected to the LAN controller 22, and an output simulated collision detect signal CDT over a line 54 also connected to the LAN controller 22. The functions of the various signals applied to, and provided by, the signal generator circuit

circuit 40 will be explained in detail hereinafter.

The LAN controller 22 is connected to the CPU 24 over signal lines 60 and 62, whereby control signals (such as interrupts) may be passed between the CPU 24 and the LAN controller 22.

It should be understood that the LAN controller 22 operates according to the CSMA/CD protocol, as set forth for example in the aforementioned IEEE 802.3 standard. As previously mentioned, the LAN controller 22 is a commercially available LAN controller device. The operation of such a controller in accordance with usage in a CSMA/CD system will now be briefly described by way of background information which is helpful as an aid to understanding the present invention. Thus, where used in a wired LAN utilizing the CSMA/CD protocol, the controller constantly monitors link activity. Whenever it senses a carrier signal on the link, the controller defers passing a data frame by deferring any pending transmission. After the carrier signal goes inactive, the controller continues to defer for an interframe spacing time configurable to a certain number of clock cycles. If, at the end of that time, it has a frame waiting to be transmitted, transmission is initiated independently of the sensed carrier. After transmission has been started, the controller attempts to transmit the entire frame. In the normal case, frame transmission is completed, and the host processor is notified. However, transmission may be terminated prematurely. This occurs, for example, when the collision detect input to the controller is activated, as will now be described. When the controller has finished deferring and has started transmission, it is still possible to experience link contention. This situation is called a collision, and it is generally detected by the transceiver, which then activates the collision detect input to the controller. The controller informs the other stations of a collision by transmitting a jam pattern, which is detected by the other stations in the LAN. The dynamics of collision handling are largely determined by a so-called "slot time". The slot time is configurable and normally based on the maximum end to end round trip delay time of the network plus jam time. Slot time is important because it is the worst case time to detect a collision. After a collision, the controller attempts to retransmit the frame after a so-called backoff time, unless the number of retransmission attempts has exceeded the maximum allowed. The controller calculates the backoff time according to the IEEE 802.3 standard: backoff is an integral number of slot times. It is a random number, from 0 to a maximum value. The maximum value is $2^R - 1$, where R is the minimum between 10 and the number of retransmission attempts. This range can be extended using an "accelerated contention resolution" mechanism. The application of this capability gives a range from 0 to a maximum value of $2^{R+K} - 1$, where K is the retry counter offset and R + K has a maximum value of 10.

It should be understood that the controller includes a retry counter which is incremented after each retransmission attempt. If retransmission is successful, the user is notified. If the number of retries exceeds the maximum, an error is reported.

Returning to the single-channel wireless LAN 10, Fig. 1, difficulties arise in an attempt to apply a CSMA/CD protocol since a station 12 which is transmitting cannot receive a signal, thereby rendering the detection of a collision difficult or impossible. However, it would be feasible to apply a CSMA technique without collision detection if the risk of collisions were small. This requires that any carrier activity has to be detected very quickly to minimize the probability that different stations start transmitting simultaneously or at times very closely spaced. The carrier detect time can be regarded as a period during which collisions can occur, and it should be small compared to the message duration. In a radio LAN, the carrier detect time has several contributions, namely transceiver delay (transmitter and receiver) and through-the-air delay. The main part of the carrier detect time (of about 30 microseconds) is contributed by the receiver, resulting from functions such as automatic gain control, correlator filter, and carrier-signal detection. The through-the-air delay at indoor distances below 300 meters is small (less than 1 microsecond). This carrier detect time is relatively long compared with a typical carrier detect of about 1 to 6 microseconds for a wired LAN. Thus, the application of a straightforward CSMA technique for a radio LAN has disadvantages.

Referring again to Fig. 2, the signal generator circuit 40 is effective to simulate a collision, thereby providing a CDT (collision detect) signal on the line 54 when a data frame transmission has been deferred, even though no actual collision has occurred. Thus, transmission of the deferred data frame is initiated only after the lapse of a random backoff time. In this manner, the risk of collisions resulting from stations 12 commencing to transmit at simultaneous or closely spaced times is considerably reduced.

With the above in mind, the signal generator circuit 40 will now be described with reference to Figs. 3A and 3B. The input line 42, which carries the TXCLK pulses is connected to an inverter 70, the output of which is connected to the count input of 4-bit counter 72 having its QD output connected over a line 74 to a 4-bit counter 76, the QB output of which is connected over a line 78 to the D input of a D-type flip-flop 90. The input line 46, which provides the carrier sense signal CRS, is connected over lines 84 and 86 to reset inputs of the counters 72 and 76, respectively. It should be understood that the devices 70, 72, and 76 together form a timer, indicated generally as 88, such that an active signal appears at the QB output of the counter 76 after a time corresponding to 32 TXCLK periods from the falling edge of the CRS signal.

The Q output of the flip-flop 90 is connected to the clock input of a D-type flip-flop 92. The clock input of the flip-flop 90 is connected over a line 94 to the input line 42. The D input of the flip-flop 92 is connected to a supply voltage V_{cc} . The input line 46 is connected to an inverter 98, the output of which is connected to the reset inputs of the flip-flops 90 and 92, over lines 100 and 102, respectively. With this arrangement, the Q output of the flip-flop 92 provides a window start signal WS on an output line 104.

The line 104 is connected to the reset input of an 8-bit shift register 106 (Fig. 3A), the clock input of which receives the TXCLK pulses over a line 108 connected to the input line 42. The outputs of the shift register 106 are connected to respective inputs of a header 109, having its outputs commonly connected to a line 110, whereby a desired one of the shift register outputs may be selected to apply a corresponding delayed signal to the output line 110. The line 110 is connected to an inverter 112 whose output on the line 114 provides an active low window end signal WE/. The WS and WE/ signals on the lines 104 and 114 are applied to an AND gate 116 (Fig. 3B), the output of which provides a window signal WD on a line 118.

The window signal WD on the line 118 is applied to an OR gate 120, the output of which is connected to the D input of a D-type flip-flop 122, the Q output of which is connected to the output line 54 to provide the simulated collision detect signal CDT. The clock input of the flip-flop 122 is connected over a line 124 to receive the TXCLK pulses from the input line 42. The reset input of the flip-flop 122 is connected over a line 126 to the input line 44 which carries the request-to-send signal RTSA.

The Q output of the flip-flop 122 (Fig. 3B) is also connected via a line 128 to an input of the OR gate 120 and to an input of an OR gate 130. Another input of the OR gate 130 is connected to the output of an AND gate 132 which has inputs connected, respectively, to the output of the inverter 98 and to the output of the inverter 112.

The input line 44 (Fig. 3A) is also connected to an inverter 134, the output of which is connected to an input of a NOR gate 136 (Fig. 3B), a second input of which is connected to the output of the OR gate 130. The output of the NOR gate 136 is connected to the output line 50 to provide the request-to-send signal RTSB.

The input line 48 is connected to an inverter 138 (Fig. 3A) the output of which is connected to an input of a NAND gate 140 (Fig. 3B) a second input of which is coupled to the Q/output of the flip-flop 122. The output of the NAND gate 140 is connected to the output line 52 to provide the clear-to-send signal CTSB.

The operation of the signal generator circuit 40 (Figs. 3A and 3B) will now be briefly described. When the carrier sense signal CRS on the line 46 drops, the timer 88 provides an active output signal on the line

78 after 32 TXCLK pulse periods, corresponding to the interframe spacing (IFS) time. The output of the timer 88 is synchronized by the flip-flop 90 to eliminate any possible voltage spikes. The CRS/ signal at the output of the inverter 98 ensures that the flip-flops 90 and 92 are enabled when the signal CRS drops. The output of the flip-flop 92 provides the window start signal WS at a time 32 TXCLK pulse periods after the CRS signal drops. When the window start signal WS on the line 104 is inactive, it resets the shift register 106. When the window start signal WS becomes active, it is delayed and inverted by the shift register 106, header 109, and inverter 112, to provide an inverted window end signal WE/ on the line 114. The WS signal on the line 104 and the WE/ signal on the line 114 are combined in the AND gate 116 to provide the window signal WD which is active for a predetermined number N of TXCLK pulse periods, where N lies between 1 and 8, and is selected by selecting a desired one of the outputs QA to QH of the shift register 106 by connecting the corresponding equal numbered pins on the header 109. In the preferred embodiment, the output QD of the shift register 106 is selected, whereby, when the window signal WD has become active, it stays active for 4 TXCLK periods.

If the signal RTSA on the line 44 becomes active during the active state of the window signal WD, the flip-flop 122 provides the signal CDT on the line 54, simulating a collision. The feedback from the flip-flop 122 on the line 128 to the OR gate 120 ensures that when the signal CDT becomes active, it stays active until the falling edge of the signal RTSA (after the controller 22 has transmitted the preamble and jam pattern).

The inverter 138 and NAND gate 140 ensure that the signal CTSA follows the signal CTSA as long as the signal CDT is not active (no simulated collision). When CDT becomes active, then the signal CTSA also becomes active independently of the signal CTSA.

The signal RTSB is produced by utilizing the inverter 134, the AND gate 132, the OR gate 130 and the NOR gate 136. Thus, the signal RTSB does not follow the signal RTSA if the signal CDT is active (simulated collision), thereby preventing transmission of the preamble and jam pattern. Also, since the signal CTSA/ from the inverter 138 is applied to the NAND gate 140 together with the output of the flip-flop 122, the signal CTSA follows the signal CTSA as long as CDT is inactive.

The operation of the station 12 will now be explained, with reference to Figs. 4A to 4C, under three operating conditions. Referring first to Fig. 4A, the waveforms shown therein relate to the situation where another station transmits a data frame, but the station 12 (Fig. 2) does not request transmission of a data frame. Under these conditions, the window signal WD is generated after the 32-bit IFS (interframe spacing)

time, but since the station 12 is not requesting to transmit a data frame, the window signal WD has no significant effect.

Referring now to Fig. 4B, the waveforms shown therein relate to the situation where the station 12 requests transmission of a data frame, but the other stations are inactive, so that the CRS signal remains at a low level. Under these conditions, the window signal WD is not generated. The request-to-send signal RTSA causes the signal generator circuit 40 to provide the request-to-send signal RTSB to the transceiver 20, which in response provides a clear-to-send signal CTSA to the signal generator circuit 40 which provides the clear-to-send signal CTSA to the LAN controller 22, whereby data frame transmission is enabled.

Referring finally to Fig. 4C, the waveforms shown therein relate to the situation where another station is transmitting a data frame, such that the signal CRS in the station 12 is active at a time when, in the station 12, the LAN controller 22 is notified that the station 12 desires to transmit a data frame. Under these conditions, transmission of the data frame in the station 12 is deferred by the controller 22. After the signal CRS becomes inactive, and following the elapse of the interframe spacing time IFS, the window signal WD is generated in the signal generator circuit 40 in the manner described hereinabove with reference to Figs. 3A and 3B. Since the controller 22 also activates the signal RTSA at this time, the signal generator circuit 40 activates the signal CDT on the line 54, to simulate a collision. This causes the controller 22 to stop its transmission after completion of sending the preamble and jam patterns. However, these patterns are not transmitted by the station 12 since the signal RTSB is not generated if a collision is simulated. Thus, the controller 22 is conditioned to the backoff mode, calculates its backoff time based on a random number of slot times, as discussed hereinabove, where the random number lies between 0 and $2^{R+K} - 1$, K being the preset retry counter offset value. After the random backoff period has expired, the controller 22 attempts to retransmit the deferred frame, as shown at the right-hand side of Fig. 4C.

It will be appreciated that, in accordance with the collision avoidance technique described herein, there is generated, after deferring a frame to be transmitted, a random waiting time before the first new transmission attempt. The total waiting time after the carrier goes inactive is composed of the interframe spacing time, the preamble and jam pattern, a second interframe spacing time, and a random number of slot time intervals between 0 and $2^{K+1} - 1$. For an exemplary collision avoidance (CA) operation, the retry counter offset value K can be set to the value 5, making collisions very unlikely. At this retry counter offset value, the probability that two controllers 22 of different stations 12, after deferring frames that arrived during the

same period of carrier activity, take the same random number is 1/64.

For the described wireless LAN there are available the following configurable parameters of the controller 22 different from the default settings: slot time, interframe spacing time, and retry counter offset. These configurable parameters have default settings corresponding the IEEE 802.3 Standard with settings for a 10 Mbps network (slot time of 512 bit-times appropriate in a wired environment with maximum delay; interframe spacing time of 96-bit-times; retry counter offset of 0). For a radio LAN operating at 2 Mbps and an end-to-end (carrier detect time) delay of 30 microseconds, shorter slot and interframe spacing times can be utilized. In the preferred embodiment, the slot time is fixed at 80 bit-times, the interframe spacing time is 32 bit-times, and the retry counter offset is 5. These settings will result after deferring in a perceptible interframe spacing time of 56 microseconds (corresponding to the duration of two interframe spacing times, the preamble pattern, and the jam pattern of the controller 22), followed by a random waiting time of between 0 and 2.52 milliseconds.

The popularity of the CSMA/CD protocol for wired LANs has resulted in the widespread availability and low cost of VLSI circuits such as CSMA/CD LAN controller chips. The CSMA/CD protocol requires the ability of a transmitting station to detect the occurrence of a transmission from another station, to be aware of the occurrence of a collision. In a radio environment, however, the difference between transmit and receive levels is too great and therefore collisions cannot be detected. Application of the CSMA/CD protocol would therefore not be possible without the loss of frames due to: (1) stations accidentally starting to transmit within the carrier detect time from each other; and (2) stations starting to transmit just after the end of another station's transmission. The present invention enables the application of CSMA/CD LAN controller chips in a radio LAN environment by providing the signal generator circuit 40 disposed between the LAN controller chip 22 and the radio transceiver 20, thereby obviating the loss of frames in situation (2) above.

Although the preferred embodiment has been described as a wireless LAN using radio frequency transmissions, it will be appreciated that in alternative embodiments, other frequencies, outside the 10 KHz to 3000 GHz radio frequency band, such as infrared frequencies, may be employed in the wireless LAN.

Claims

1. A method of communicating among at least two data processing stations (12) coupled by a wireless LAN (10) operating over a wireless transmission channel, characterized by the steps of:

providing a controller chip (22) which is designed for use with a CSMA/CD protocol in a wired LAN; generating a control signal (RTSA) at a predetermined time by a data processing station (12) wishing to transmit; using said control signal (RTSA) to activate a collision detect input of said controller chip (22); and using a random delay time determined in said controller chip (22) to initiate transmission by said data processing station (12) wishing to transmit.

2. A method according to claim 1, characterized by the steps of: monitoring said wireless transmission channel to detect the end of a data transfer thereover; generating a window signal (WD) dependent upon said end of said data transfer; generating a collision detect signal (CDT) if said control signal (RTSA) is active during said window signal (WD); using said CDT signal to initiate a random delay time assigned to the data processing station (12); and initiating transmission by the data processing station (12) generating said CDT signal at the end of the delay time assigned thereto.
3. A local area network station, including memory means (26) adapted to store data to be transmitted, and communication controller means (22) adapted to control the transmission of data frames by said station (12); and transceiver means (20), characterized in that said transceiver means (20) is adapted to operate on a single wireless transmission channel, in that said communication controller means (22) is adapted to defer transmission of a data frame in response to a first control signal (CRS) applied thereto and is further effective, in response to a second control signal (CDT) applied thereto, to terminate the transmission of a data frame which is being transmitted and to reinstate transmission thereof after a back-off period; and in that signal generating means (40) is provided, coupled to said transceiver means (20) and to said communication controller means (22) and adapted, in response to the outputting by said communication controller means (22) of a third control signal (RTSA) requesting transmission of a deferred data frame, to generate said second control signal (CDT) thereby causing said communication controller means (22) to inhibit transmission of the deferred data frame until said backoff period has elapsed.
4. A local area network station according to claim 3, characterized in that said signal generating means (40) includes window signal generating means (88, 90, 92, 98, 106, 109, 112, 116) adapted to generate a window signal (WD) in response to the termination of said first control signal

(CRS), and first logic circuit means (120, 122) responsive to said window signal (WD) and to said third control signal (RTSA), and adapted to provide said second control signal (CDT).

- 5
5. A local area network according to claim 4, characterized in that said window signal generating means includes timer means (88) having an output connected to second logic circuit means (90,92) responsive to provide a window start signal (WS) a first predetermined time after the termination of said first control signal (CRS), third logic circuit means (106,109,112) adapted to provide a window end signal (WE/) a second predetermined time after the initiation of said window start signal (WS), and fourth logic circuit means (116) responsive to said window start signal (WS) and said window end signal (WE/) to provide said window signal (WD). 10 15
- 20
6. A local area network station according to claim 5 characterized in that said third logic circuit means includes: a shift register (106) having an input coupled to an output (104) of said second logic circuit means (90,92); and a header device (109) having a plurality of inputs coupled to a corresponding plurality of outputs of said shift register (106), and a plurality of outputs coupled to a common line (110), whereby the time for which said window signal (WD) is active may be selected by selective connection between a selected input and a selected output of said header device (109). 25 30
- 35
7. A local area network station according to claim 5 or claim 6 characterized in that said signal generating means (40) includes fifth logic circuit means (130,136) responsive to said second control signal (CDT) and said third control signal (RTSA) to provide a fourth control signal (RTSB) applied to said transceiver (20), said fourth control signal (RTSB) being indicative of a request-to-send condition and being inhibited if said second control signal (CDT) is active. 40 45
- 50
8. A local area network station according to claim 7 characterized in that said signal generating means (40) includes sixth logic circuit means (138, 140) responsive to said second control signal (CDT) and arranged to receive a fifth control signal (CTSA) provided by said transceiver means (20) and indicative of a clear-to-send condition in said transceiver means (20), said sixth logic circuit means (138,140) being adapted to provide a sixth control signal (CTSB) to said communication controller means (22) when said fifth control signal (CTSA) is active or when said second control signal (CDT) is active. 55

FIG. 1

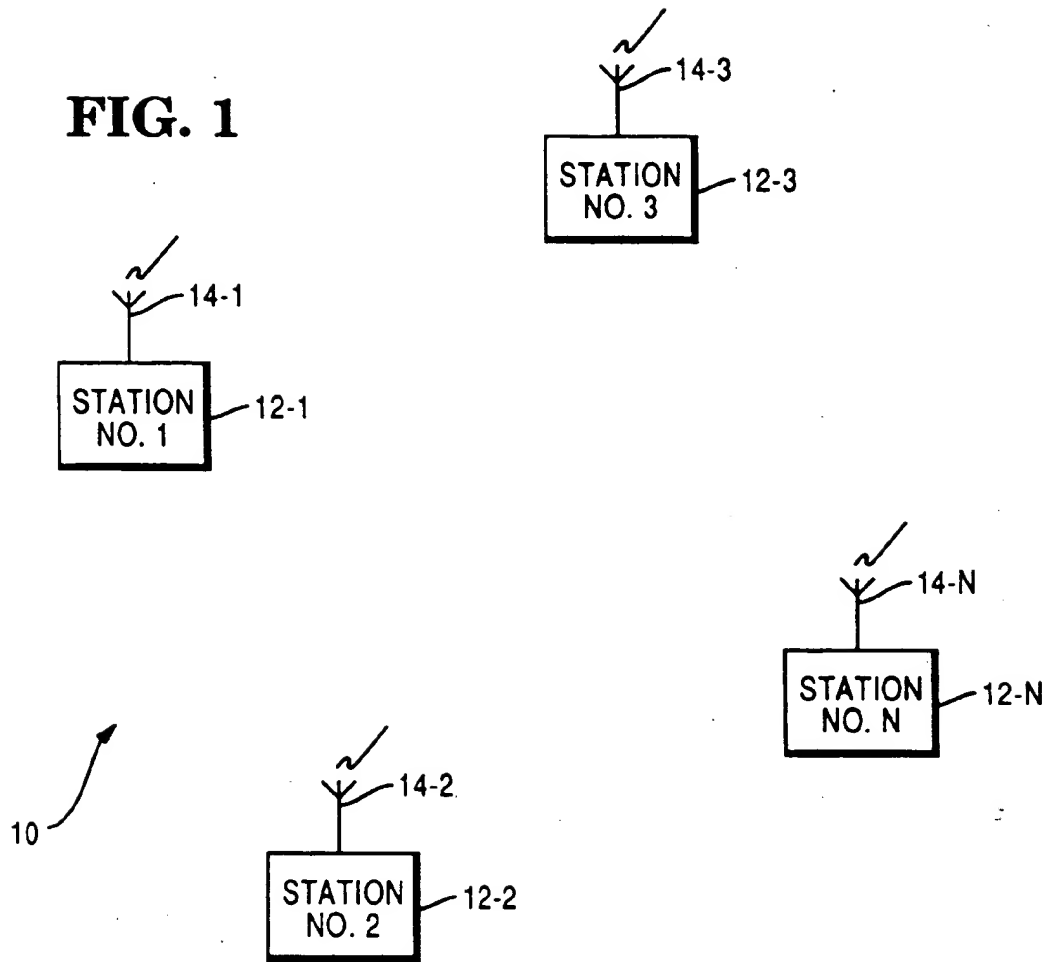


FIG. 4C

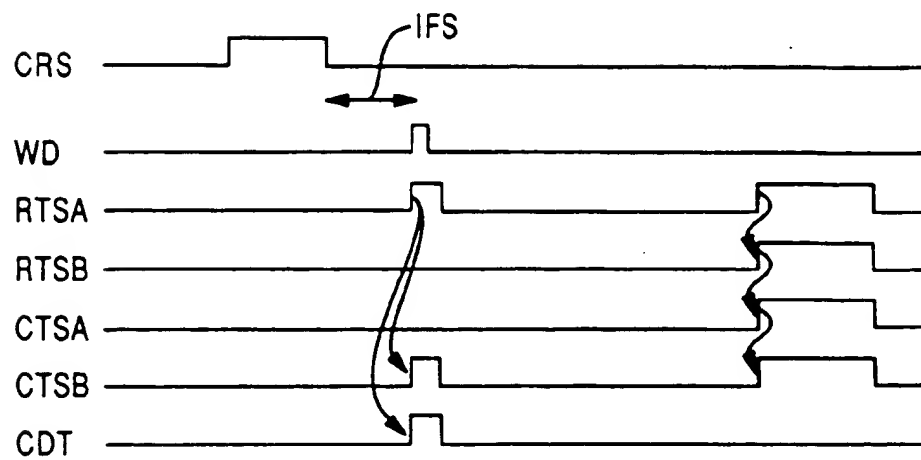


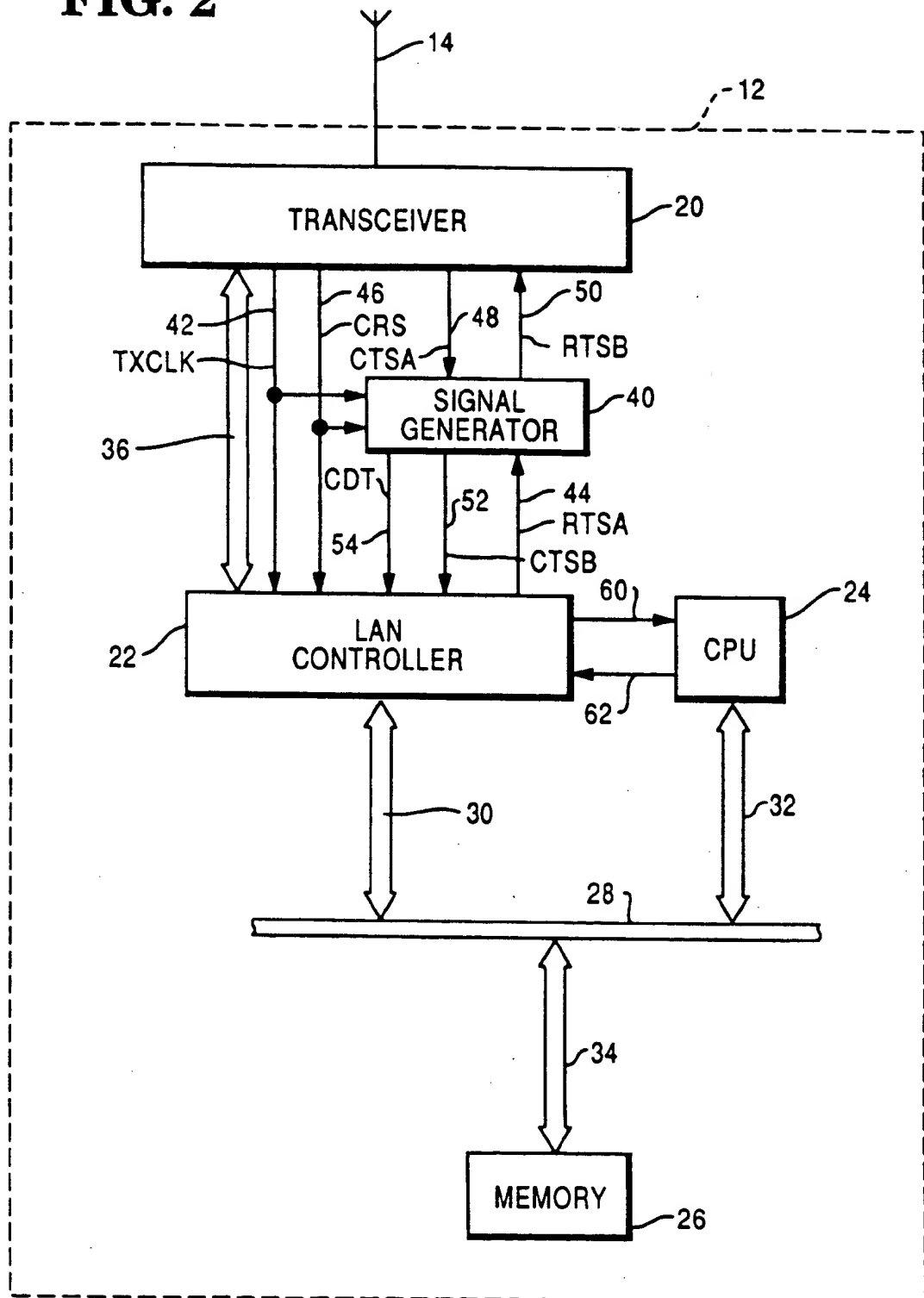
FIG. 2

FIG. 3A

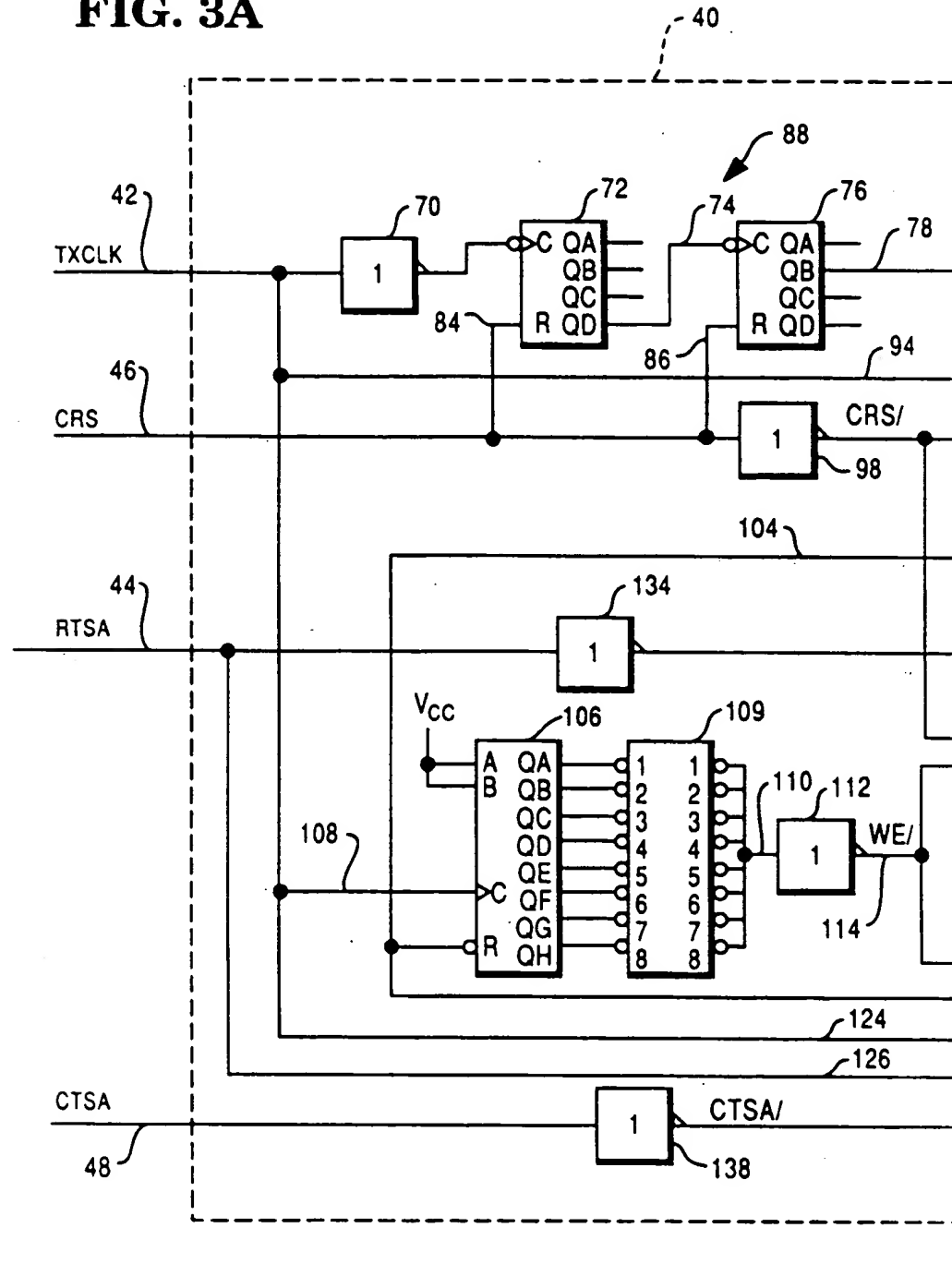


FIG. 3B

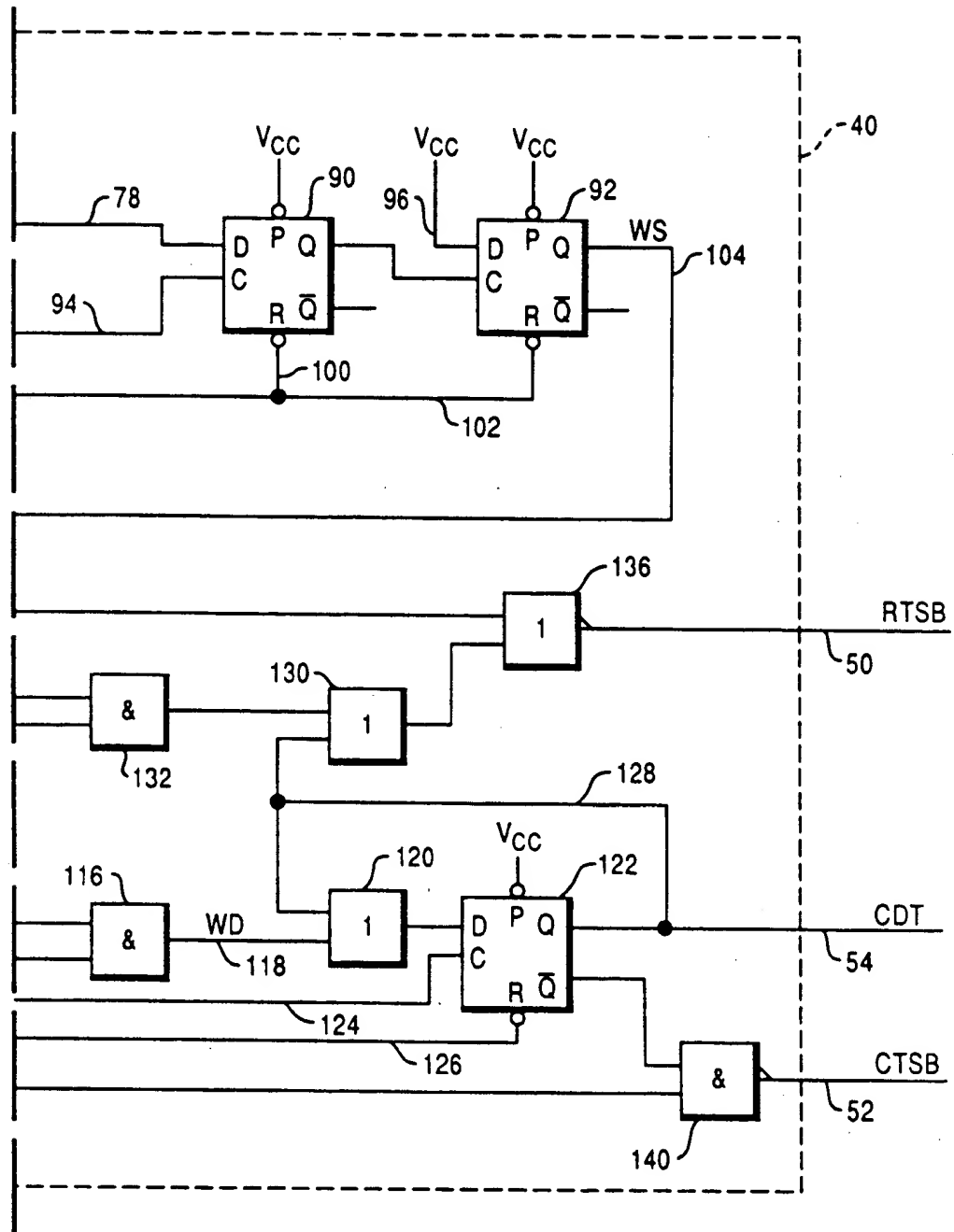


FIG. 4A

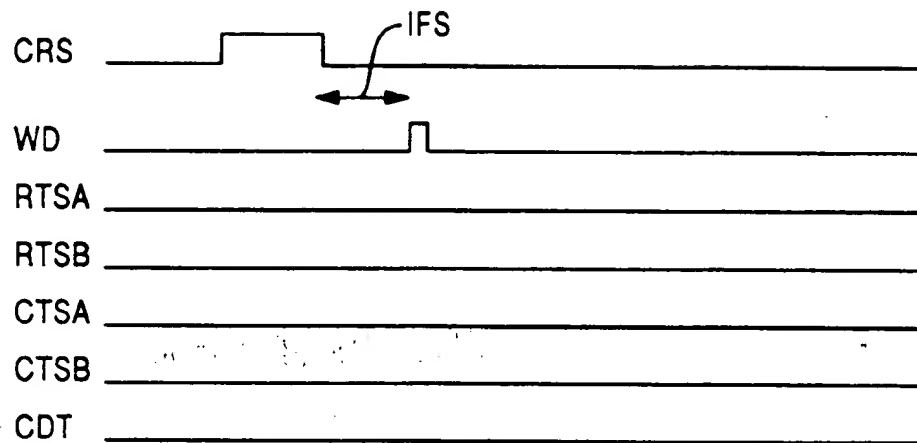
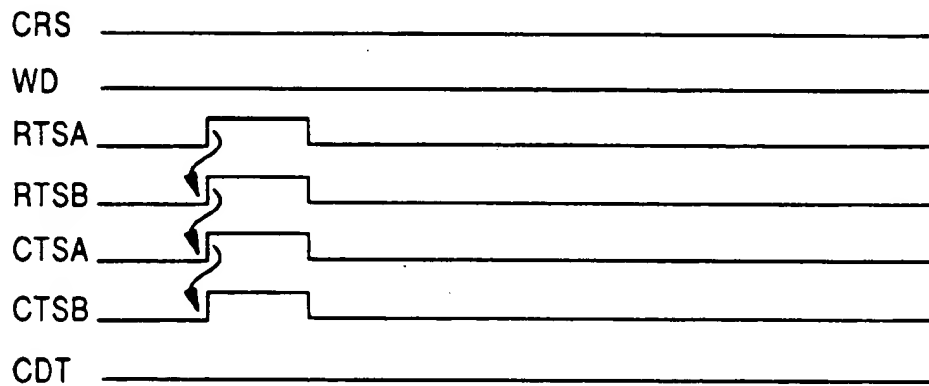


FIG. 4B



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